

What is claimed is:

1 1. A mechanism for preventing ESD damage to a
2 electronic device comprising at least one connection area
3 having a plurality of pads (P_1 to P_n) arranged
4 sequentially for mounting to an integrated circuit, and a
5 plurality of fan-out signal lines (F_1 to F_n) extending
6 from the pads (P_1 to P_n) respectively, the pads P_1 and P_n
7 disposed on outermost sides of the connection area, the
8 mechanism comprising:

9 a plurality of ESD protection device (ES_1 to ES_n)
10 configured corresponding to the fan-out signal
11 lines (F_1 to F_n);

12 wherein, equivalent impedances of the ESD protection
13 devices ES_1 and ES_n are smaller than equivalent
14 impedances of the other ESD protection devices
15 ES_2 to ES_{n-1} .

1 2. The mechanism as claimed in claim 1, wherein
2 each ESD protection device comprises at least one element
3 having a MOS transistor circuit structure and equivalent
4 channel widths of the ESD protection devices ES_1 and ES_n
5 are longer than equivalent channel widths of the other
6 ESD protection devices ES_2 to ES_{n-1} .

1 3. A mechanism for preventing ESD damage to a
2 electronic device comprising at least one connection area
3 having a plurality of pads (P_1 to P_n) arranged
4 sequentially for mounting to an integrated circuit, and a
5 plurality of fan-out signal lines (F_1 to F_n) extending
6 from the pads (P_1 to P_n) respectively, the pads P_1 and P_n

7 disposed on outermost sides of the connection area, the
8 mechanism comprising:

9 a plurality of ESD protection device (ES_1 to ES_n)
10 configured corresponding to the fan-out signal
11 lines (F_1 to F_n);

12 wherein, equivalent impedances of the ESD protection
13 devices ES_1 to ES_j gradually increase and
14 equivalent impedances of the ESD protection
15 devices ES_{j+1} to ES_n gradually decrease, $1 < j < n$.

1 4. The mechanism as claimed in claim 3, wherein
2 each ESD protection device comprises at least one element
3 having a MOS transistor circuit structure, equivalent
4 channel widths of the ESD protection devices ES_1 to ES_j
5 gradually decrease, and equivalent channel widths of the
6 ESD protection devices ES_{j+1} to ES_n gradually increase.

1 5. A mechanism for preventing ESD damage to a
2 electronic device comprising at least one connection area
3 having a plurality of pads (P_1 to P_n) arranged
4 sequentially for mounting to an integrated circuit, and a
5 plurality of fan-out signal lines (F_1 to F_n) extending
6 from the pads (P_1 to P_n) respectively, the pads P_1 and P_n
7 disposed on outermost sides of the connection area, the
8 mechanism comprising:

9 a plurality of ESD protection device (ES_1 to ES_n)
10 configured corresponding to the fan-out signal lines (F_1
11 to F_n);

12 wherein, an equivalent impedance of one ESD
13 protection device ES_k is different from equivalent
14 impedances of the other ESD protection devices, $1 \leq k \leq n$.

1 6. The mechanism as claimed in claim 5, wherein
2 each ESD protection device comprises at least one element
3 having a MOS transistor circuit structure and an
4 equivalent channel width of the ESD protection device ES_k
5 is different from equivalent channel widths of the other
6 ESD protection devices.

1 7. A liquid crystal display panel, comprising:
2 a pixel array;
3 at least one connection area having a plurality of
4 pads (P_1 to P_n) arranged sequentially for
5 mounting to an integrated circuit, wherein the
6 pads P_1 and P_n are disposed on outermost sides
7 of the connection area;
8 a plurality of fan-out signal lines (F_1 to F_n)
9 extending from the pads (P_1 to P_n)
10 respectively; and
11 a plurality of ESD protection devices (ES_1 to ES_n)
12 configured corresponding to the fan-out signal
13 lines (F_1 to F_n);
14 wherein, equivalent impedances of the ESD protection
15 devices ES_1 and ES_n are smaller than equivalent
16 impedances of the other ESD protection devices
17 ES_2 to ES_{n-1} .

1 8. The liquid crystal display panel as claimed in
2 claim 7, wherein each ESD protection device comprises at

least one element having a MOS transistor circuit structure and equivalent channel widths of the ESD protection devices ES_1 and ES_n are longer than equivalent channel widths of the other ESD protection devices ES_2 to ES_{n-1} .

9. The liquid crystal display panel as claimed in claim 8, wherein the equivalent channel widths of the ESD protection devices ES_1 to ES_j gradually decrease, and the equivalent channel widths of the ESD protection devices ES_{j+1} to ES_n gradually increase, $1 < j < n$.

10. A liquid crystal display panel, comprising:
a pixel array;
at least one connection area having a plurality of pads (P_1 to P_n) arranged sequentially for mounting to an integrated circuit, wherein the pads P_1 and P_n are disposed on outermost sides of the connection area;
a plurality of fan-out signal lines (F_1 to F_n) extending from the pads (P_1 to P_n) respectively; and
a plurality of ESD protection device (ES_1 to ES_n) configured corresponding to the fan-out signal lines (F_1 to F_n);

wherein, an equivalent impedance of one ESD protection device ES_k is different from equivalent impedances of the other ESD protection devices, $1 \leq k \leq n$.

11. The liquid crystal display panel as claimed in claim 10, wherein each ESD protection device comprises at

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3 least one element having a MOS transistor circuit
4 structure and an equivalent channel width of the ESD
5 protection device ES_k is different from equivalent channel
6 widths of the other ESD protection devices.